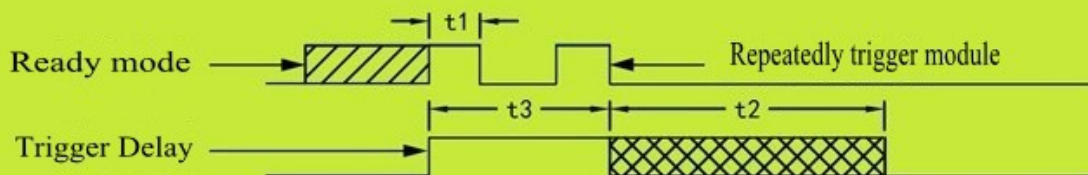


Delay module $t=t1(\text{Trigger time})+t2(\text{Chip delay time})$



Module delay $t = t3 (\text{multiple trigger time and interrupt latency time})+t2(\text{Chip delay time})$

S1位置	S2位置	不插S4时间	插上S4时间	图示
0	1	0.13S-1.3S	1.5S-14.5S	
1	0	0.5S-5.2S	6S-58S	
0	0	4.4S-42S	48S-463S	
1	1	38S-340S	389S-3700S	